CLAIMS

1. A sensing circuit, comprising:

an integrator circuit having a first integrator input electrically coupled to a reference level, a second integrator input to which an input is applied, and first and second integrator outputs at which first and second output signals are provided, respectively, the integrator circuit further having an amplifier circuit having pairs of differential input and output nodes, the integrator circuit periodically switching the electrical coupling of each of the differential input nodes to a respective integrator input and the electrical coupling of each of the differential output nodes to a respective integrator output;

a comparator having first and second input nodes electrically coupled to a respective integrator output and further having an output node, the clocked comparator periodically comparing voltage levels of the first and second input nodes and generating an output signal having a logic state based therefrom; and

a current source having first and second current output nodes coupled to a respective integrator output, the current source switching the coupling of each current output node to a integrator output based on the logic state of the output signal of the comparator.

2. The sensing circuit of claim 1 wherein the period at which the integrator circuit switches the coupling of the differential input and output nodes is greater than the period at which the comparator compares the voltage levels of the first and second input nodes.

3. The sensing circuit of claim 1 wherein the comparator comprises:

a clocked latch having a pair of complementary data nodes, first and second input terminals coupled to a respective integrator output, the clocked latch latching data states applied to the first and second input terminals; and

a flip-flop electrically coupled to the complementary data nodes for providing an output signal indicative of the latched data states.

4. The sensing circuit of claim 3 wherein the clocked latch latches the data states at its first and second input terminals for a first half of the period at which the comparator compares voltage levels, and the clocked latch is set to a reference voltage level for a second half of the period.

5. The sensing circuit of claim 1 wherein the integrator circuit comprises:

a first switching circuit having a first pair of switches for electrically coupling the first integrator input to the first differential input and the second integrator input to the second differential input, and a second pair of switches for electrically coupling the first integrator input to the second differential input and the second integrator input to the first differential input; and

a second switching circuit having a first pair of switches for electrically coupling the first differential output to the first integrator output and the second differential output to the second integrator output, and a second pair of switches for electrically coupling the first differential output to the second integrator output and the second differential output to the first integrator output.

6. The sensing circuit of claim 5 wherein the first pairs of switches of the first and second switching circuits are activated for the first half of the period at which the integrator circuit switches the coupling, and the second pairs of switches of the first and second switching circuits are activated for the second half of the period.

7. The sensing circuit of claim 1, further comprising a feedback stage electrically coupled to the first and second integrator outputs and the amplifier circuit, the feedback stage adjusting output current of the amplifier circuit based on the relative voltage levels of the first and second integrator outputs.

8. A sensing circuit having a sensing node electrically coupled to a memory cell and reference node electrically coupled to a reference level, the sensing circuit comprising:

a differential amplifier having first and second differential input and output nodes;

a switching circuit having first and second switching input and output terminals, and a clock node at which a first clock signal is applied, the switching circuit electrically coupled to the differential input and output nodes and, in accordance with the first clock signal, switching the coupling of the first and second switching input nodes to a respective differential input node and switching the coupling of the first and second switching output nodes to a respective differential output node;

first and second capacitors electrically coupled to a respective switching output node;

a clocked comparator having an output node, a clock node at which a second clock signal is applied, and first and second input nodes electrically coupled to a respective capacitor, in response to the second clock signal, the clocked comparator generating an output signal having a logic state based on the relative voltage levels of the first and second capacitors; and

a current source having first and second current output nodes electrically coupled to a respective capacitor, the current source switching the coupling of each current output node to a respective capacitor based on the logic state of the output signal of the clocked comparator.

9. The sensing circuit of claim 8, further comprising a feedback stage electrically coupled to the first and second capacitors and the differential amplifier, the feedback stage adjusting output current of the differential amplifier based on the relative voltage levels of the first and second capacitors.

10. The sensing circuit of claim 8 wherein the clocked comparator comprises:

a clocked latch having a pair of complementary data nodes, first and second input terminals electrically coupled to a respective capacitor, and a clock node at which the second clock signal is applied; and

a flip-flop electrically coupled to the complementary data nodes for providing an output signal indicative of the data states of the complementary data nodes.

11. The sensing circuit of claim 8 wherein the first clock signal has a frequency greater than the second clock signal.

12. The sensing circuit of claim 8, further comprising an integrator circuit having a pair of integrator input nodes and a pair of integrator output nodes, the integrator circuit electrically interposed between the first and second capacitors and the clocked comparator, each integrator input node of the pair electrically coupled to a respective capacitor and each integrator output node of the pair electrically coupled to a respective input node of the clocked comparator.

13. A sensing circuit, comprising:

a first integrator circuit having a first integrator input electrically coupled to a reference level, a second integrator input to which an input is applied, and first and second integrator outputs at which first and second output signals are provided, respectively, the integrator circuit further having an amplifier circuit having pairs of differential input and output nodes, the integrator circuit periodically switching the electrical coupling of each of the differential input nodes to a respective integrator input and the electrical coupling of each of the differential output nodes to a respective integrator output;

a second integrator circuit having first and second integrator inputs coupled to a respective integrator output of the first integrator circuit and first and second integrator outputs;

a comparator having first and second input nodes electrically coupled to a respective integrator output of the second integrator circuit and further having an output node, the clocked comparator periodically comparing voltage levels of the first and second input nodes and generating an output signal having a logic state based therefrom; and

a current source having a first pair of current output nodes coupled to a respective integrator output of the first integrator circuit, and further having a second pair of current output nodes coupled to a respective integrator output of the second integrator circuit, the current source switching the coupling of each current output node of the first pair to a respective integrator output of the first integrator circuit, and each current output node of the second pair to a respective integrator output of the second integrator circuit based on the logic state of the output signal of the comparator.

14. The sensing circuit of claim 13 wherein the period at which the first integrator circuit switches the coupling of the differential input and output nodes is greater than the period at which the comparator compares the voltage levels of the first and second input nodes.

15. The sensing circuit of claim 13 wherein the comparator comprises:

a clocked latch having a pair of complementary data nodes, first and second input terminals coupled to a respective integrator output of the second integrator, the clocked latch latching data states applied to the first and second input terminals; and

a flip-flop electrically coupled to the complementary data nodes for providing an output signal indicative of the latched data states.

16. The sensing circuit of claim 13 wherein the clocked latch latches the data states at its first and second input terminals for a first half of the period at which the comparator compares voltage levels, and the clocked latch is set to a reference voltage level for a second half of the period.

17. The sensing circuit of claim 13 wherein the first integrator circuit comprises:

a first switching circuit having a first pair of switches for electrically coupling the first integrator input to the first differential input and the second integrator input to the second differential input, and a second pair of switches for electrically coupling the first integrator input to the second differential input and the second integrator input to the first differential input; and

a second switching circuit having a first pair of switches for electrically coupling the first differential output to the first integrator output and the second differential output to the second integrator output, and a second pair of switches for electrically coupling the first differential output to the second integrator output and the second differential output to the first integrator output.

18. The sensing circuit of claim 17 wherein the first pairs of switches of the first and second switching circuits are activated for the first half of the period at which the integrator circuit switches the coupling, and the second pairs of switches of the first and second switching circuits are activated for the second half of the period.

19. The sensing circuit of claim 13 wherein the first integrator circuit further comprising a feedback stage electrically coupled to the first and second integrator outputs of the first integrator and the amplifier circuit, the feedback stage adjusting output current of the amplifier circuit based on the relative voltage levels of the first and second integrator outputs of the first integrator circuit.

20. A memory device, comprising:

an address bus;

a control bus;

a data bus;

an address decoder coupled to the address bus;

a control circuit coupled to the control bus;

an MRAM array coupled to the address decoder and control circuit, the MRAM array having a plurality of word lines, a plurality of bit lines, a plurality of memory cells arranged in rows and columns, each memory cell in a respective row being coupled to a corresponding word line and each memory cell in respective column being coupled to a corresponding bit line; and;

a read/write circuit coupled to the data bus and the MRAM array, the read/write circuit including sensing circuits coupled to the bit lines, each sensing circuit comprising:

an integrator circuit having a first integrator input electrically coupled to a reference level, a second integrator input coupled to a respective bit line, and first and second integrator outputs at which first and second output signals are provided, respectively, the integrator circuit further having an amplifier circuit having pairs of differential input and output nodes, the integrator circuit periodically switching the electrical coupling of each of the differential input nodes to a respective integrator input and the electrical coupling of each of the differential output nodes to a respective integrator output;

a comparator having first and second input nodes electrically coupled to a respective integrator output and further having an output node, the clocked comparator periodically comparing voltage levels of the first and second input nodes and generating an output signal having a logic state based therefrom; and

a current source having first and second current output nodes coupled to a respective integrator output, the current source switching the coupling of each current output node to a integrator output based on the logic state of the output signal of the comparator.

21. The memory device of claim 20 wherein the period at which the integrator circuit in the sensing circuit switches the coupling of the differential input and output nodes is greater than the period at which the comparator compares the voltage levels of the first and second input nodes.

22. The memory device of claim 20 wherein the comparator of the sensing circuit comprises:

a clocked latch having a pair of complementary data nodes, first and second input terminals coupled to a respective integrator output, the clocked latch latching data states applied to the first and second input terminals; and

a flip-flop electrically coupled to the complementary data nodes for providing an output signal indicative of the latched data states.

23. The memory device of claim 22 wherein the clocked latch of the sensing circuit latches the data states at its first and second input terminals for a first half of the period at which the comparator compares voltage levels, and the clocked latch is set to a reference voltage level for a second half of the period.

24. The memory device of claim 20 wherein the integrator circuit of the sensing circuit comprises:

a first switching circuit having a first pair of switches for electrically coupling the first integrator input to the first differential input and the second integrator input to the second differential input, and a second pair of switches for electrically coupling the first integrator input to the second differential input and the second integrator input to the first differential input; and

a second switching circuit having a first pair of switches for electrically coupling the first differential output to the first integrator output and the second differential output to the second integrator output, and a second pair of switches for electrically coupling the first differential output to the second integrator output and the second differential output to the first integrator output.

25. The memory device of claim 24 wherein the first pairs of switches of the first and second switching circuits are activated for the first half of the period at which the

integrator circuit switches the coupling, and the second pairs of switches of the first and second switching circuits are activated for the second half of the period.

26. The memory device of claim 20 wherein the sensing circuit further comprises a feedback stage electrically coupled to the first and second integrator outputs and the amplifier circuit, the feedback stage adjusting output current of the amplifier circuit based on the relative voltage levels of the first and second integrator outputs.

27. The memory device of claim 20 wherein the integrator circuit is a first integrator circuit, and the sensing circuit further comprises a second integrator circuit having a pair of integrator input nodes and a pair of integrator output nodes, the second integrator circuit electrically interposed between the first and second integrator outputs of the first integrator circuit and the comparator, each integrator input node of the pair electrically coupled to a respective integrator output of the first integrator circuit and each integrator output node of the pair electrically coupled to a respective input node of the comparator.

28. A computer system, comprising:

a data input device;
a data output device;
a processor coupled to the data input and output devices; and
a memory device coupled to the processor, the memory device comprising,
    an address bus;
    a control bus;
    a data bus;
    an address decoder coupled to the address bus;
    a control circuit coupled to the control bus;
    an MRAM array coupled to the address decoder and control circuit, the MRAM array having a plurality of word lines, a plurality of bit lines, a plurality of memory cells

arranged in rows and columns, each memory cell in a respective row being coupled to a corresponding word line and each memory cell in respective column being coupled to a corresponding bit line; and;

a read/write circuit coupled to the data bus and the MRAM array, the read/write circuit including sensing circuits coupled to the bit lines, each sensing circuit comprising:

an integrator circuit having a first integrator input electrically coupled to a reference level, a second integrator input coupled to a respective bit line, and first and second integrator outputs at which first and second output signals are provided, respectively, the integrator circuit further having an amplifier circuit having pairs of differential input and output nodes, the integrator circuit periodically switching the electrical coupling of each of the differential input nodes to a respective integrator input and the electrical coupling of each of the differential output nodes to a respective integrator output;

a comparator having first and second input nodes electrically coupled to a respective integrator output and further having an output node, the clocked comparator periodically comparing voltage levels of the first and second input nodes and generating an output signal having a logic state based therefrom; and

a current source having first and second current output nodes coupled to a respective integrator output, the current source switching the coupling of each current output node to a integrator output based on the logic state of the output signal of the comparator.

29. The computer system of claim 28 wherein the period at which the integrator circuit in the sensing circuit switches the coupling of the differential input and output nodes is greater than the period at which the comparator compares the voltage levels of the first and second input nodes.

30. The computer system of claim 28 wherein the comparator of the sensing circuit comprises:

a clocked latch having a pair of complementary data nodes, first and second input terminals coupled to a respective integrator output, the clocked latch latching data states applied to the first and second input terminals; and

a flip-flop electrically coupled to the complementary data nodes for providing an output signal indicative of the latched data states.

31. The computer system of claim 30 wherein the clocked latch of the sensing circuit latches the data states at its first and second input terminals for a first half of the period at which the comparator compares voltage levels, and the clocked latch is set to a reference voltage level for a second half of the period.

32. The computer system of claim 28 wherein the integrator circuit of the sensing circuit comprises:

a first switching circuit having a first pair of switches for electrically coupling the first integrator input to the first differential input and the second integrator input to the second differential input, and a second pair of switches for electrically coupling the first integrator input to the second differential input and the second integrator input to the first differential input; and

a second switching circuit having a first pair of switches for electrically coupling the first differential output to the first integrator output and the second differential output to the second integrator output, and a second pair of switches for electrically coupling the first differential output to the second integrator output and the second differential output to the first integrator output.

33. The computer system of claim 32 wherein the first pairs of switches of the first and second switching circuits are activated for the first half of the period at which the

integrator circuit switches the coupling, and the second pairs of switches of the first and second switching circuits are activated for the second half of the period.

34. The computer system of claim 28 wherein the sensing circuit further comprises a feedback stage electrically coupled to the first and second integrator outputs and the amplifier circuit, the feedback stage adjusting output current of the amplifier circuit based on the relative voltage levels of the first and second integrator outputs.

35. The computer system of claim 28 wherein the integrator circuit of the sensing circuit is a first integrator circuit, and the sensing circuit further comprises a second integrator circuit having a pair of integrator input nodes and a pair of integrator output nodes, the second integrator circuit electrically interposed between the first and second integrator outputs of the first integrator circuit and the comparator, each integrator input node of the pair electrically coupled to a respective integrator output of the first integrator circuit and each integrator output node of the pair electrically coupled to a respective input node of the comparator.

36. A method of sensing a data state of a memory cell, comprising:

coupling input and output terminals of an integrator circuit according to a first configuration for a first portion of a first time period;

coupling the input and output terminals of the integrator circuit according to a second configuration for a second portion of the first time period; the second configuration changing polarity of the integrator circuit from the first configuration;

based on voltage levels at the output terminals of the integrator circuit, generating a clocked output signal representative of a value; and

averaging the value of the clocked output signal over a second time period.

37. The method of claim 36, further comprising amplifying the voltage levels at the output terminals of the integrator circuit prior to generating a clocked output signal.

38. The method of claim 36 wherein the first portion and the second portion of the first time period are equal.

39. The method of claim 36, further comprising:

providing a first current having a first polarity to a first of the output terminals of the integrator circuit and providing a second current having a second polarity opposite the first polarity to a second of the output terminals of the integrator circuit; and

switching the provision of the first and second currents to the first and second output terminals of the integrator circuit based on the value of the clocked output signal.

40. The method of claim 36 wherein the second time period is greater than and a multiple of the first time period.

41. A method of sensing a data state of a memory cell, comprising:

periodically switching coupling of input terminals and output terminals of an integrator circuit from a first configuration to a second configuration, the second configuration changing polarity of the integrator circuit from the first configuration;

periodically comparing output signals provided by the integrator circuit;

based on the comparison, generating an output signal having a voltage representative of a value; and

averaging the value of the output signal over a time period.

42. The method of claim 41, further comprising amplifying the output signals provided by the integrator signal prior to the periodic comparison.

43. The method of claim 41, further comprising:

providing a first current having a first polarity to a first of the output terminals of the integrator circuit and providing a second current having a second polarity opposite the first polarity to a second of the output terminals of the integrator circuit; and

switching the provision of the first and second currents to the first and second output terminals of the integrator circuit based on the value of the output signal.

44. The method of claim 41 wherein the switching occurs at a period greater than at which the comparing occurs.

45. The method of claim 44 wherein the period of the switching is a multiple of that at which the comparing occurs.